WHAT IS CLAIMED IS:

1. A device for creating timing constraints for a semiconductor integrated circuit designed using a hierarchical design, the device comprising:

a datapath extraction unit that extracts datapaths on which a timing verification is to be performed, wherein the datapath extraction unit extracts the datapaths, which are established between at least two child blocks in a parent block, from a cell library that includes description of logic function and timing information of each cell in the parent block, timing constraints that includes definitions of any clocks of the semiconductor integrated circuit, and a netlist that includes connection information between the cells;

a datapath output unit that creates a datapath list which allows a user to selectively specify a timing exception corresponding to the datapath extracted, and displays the datapath list for the user; and

a timing constraints modification unit that creates new timing constraints by modifying existing timing constraints based on the timing exception specified by the user.

2. The device according to claim 1, wherein the datapath extraction unit extracts only the datapath specified by the user.

3. The device according to claim 1, wherein the datapath output unit creates the datapath list of only the datapath specified by the user.

4. The device according to claim 1, wherein the datapath output unit appends a result of a timing verification to each datapath in the datapath list.

5. The device according to claim 4, wherein the datapath extraction unit extracts only the datapath having a timing error.

6. The device according to claim 1, wherein the datapath output unit creates the datapath list of only the datapath having a timing error.

7. The device according to claim 1, wherein the datapath output unit creates the datapath list of datapath for which a result of timing verification is within a predetermined range.

8. The device according to claim 1, wherein the datapath extraction unit extracts the datapath for which a result of timing verification is within a predetermined range.

9. The device according to claim 1, wherein the datapath output unit appends a clock relation to be specified as the timing exception to the datapath list, the clock relation being a relation between clocks input to the cells.

10. The device according to claim 1, wherein the datapath output unit appends a block relation to be specified as the timing exception to

the datapath list, the block relation being a relation between the child blocks.

11. The device according to claim 2, wherein the user specifies the datapath that performs transfer of data between the child blocks.

12. The device according to claim 3, wherein the user specifies the datapath that performs transfer of data between the child blocks.

13. The device according to claim 2, wherein the user specifies the datapath that performs transfer of data from one of the child blocks to other child block.

14. The device according to claim 3, wherein the user specifies the datapath that performs transfer of data from one of the child blocks to other child block.